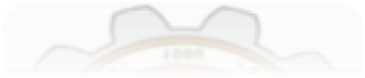
# Lab 5



**DSD Lab**

**Spring 2023**

**Submitted by:**

**Maaz Habib**

**Registration no.:**

**[20Pwcse1952]**

“On my honor, as a student of University of Engineering and Technology Peshawar, I have neither nor received unauthorized assistance on this academic work”

**Submitted to:**

**Engr:Muhammad Usman**

**LAB 5 Implementation of ROM in Xilinx**

# Objectives

Objectives of this lab are to get familiar with

* How to implement gates in XILINIX
* Observe the result on FPGA

# FPGA

FPGAs are programmable digital logic circuits. It can be programmed to do almost any digital function. There are at least 5 companies making FPGAs in the world. Xilinx is the biggest name in the FPGA world.

The FPGA kits available in our labs are SPARTAN-6 STARTER KIT BOARD.

# XILINX

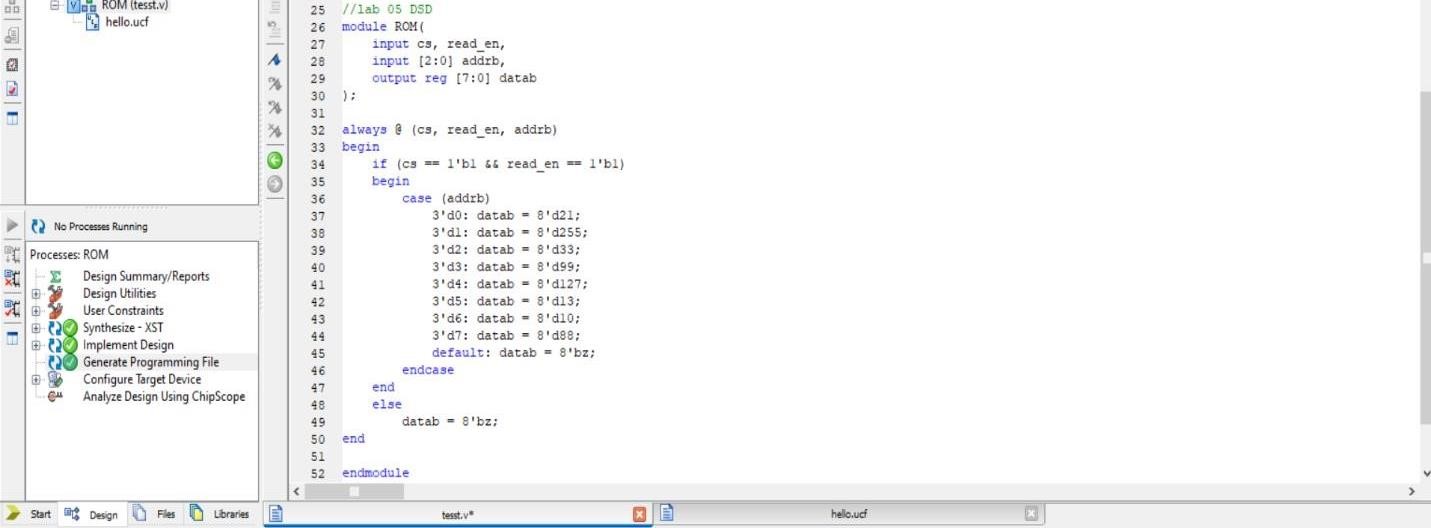
The Integrated Software Environment (ISE™) is the Xilinx® design software suite that allows us to take our design from design entry through Xilinx device programming.

# Steps

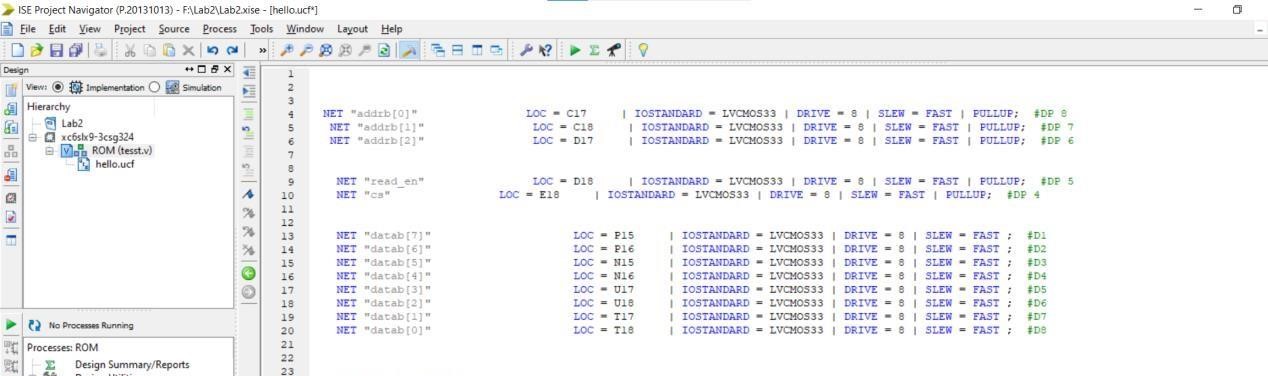
We perform following task by using following steps:

1. First of all the USER DEFINED CONSTRAINT file is created and added in the Project
2. Code is then synthesized.
3. Design is implemented.
4. Programming file is then generated which can be downloaded into the FPGA.

**Task Verilog Code**

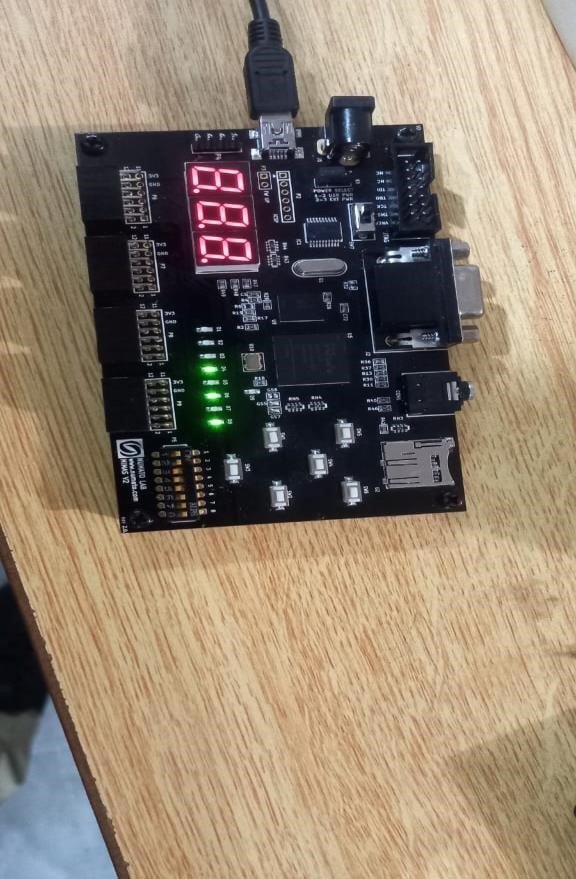


**Design Implementation**



**Outputs:**

**Output for D0=21**



**Output for D4=127**

